Diagnosis of Coarse Grain Model for Power Switches

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Abstract – Power gating technology is used in power switches for reducing leakage power. Power switches are divided in to segments, which uses DML gates. Dual mode logic gate use both dynamic and static operation. Faulty power switch is detected from segments hence achieve better diagnosis accuracy. The proposed diagnosis has been validated through number of ISCAS benchmarks. In the presence of temperature voltage and process variation, this DFT solution provides efficient testing of power switches ,to achieve faster operation DML gates are used. Finally it will be implemented using FPGA kit.

Index Terms — DML(dual mode logic),power gating, DFT(design for test)power switches.

1. INTRODUCTION

Nowadays leakage current is a major problem in many digital circuits. Power gating technique reduces leakage power. By power down the logic block during idle mode for reduction of leakage power. Power switches are usually implemented in two methods; they are fine grain or coarse grain. The main problem in fine grain method is high area over head compared with coarse grain and also it is more sensitive to voltage, temperature, process variation changes.

There for coarse grain design style is most commonly used power switches can be implemented in two modes one is completely off mode other one is intermediate power off mode. This work fully concentrate on completely power off mode.DML means dual mode logic gate, there are two modes of operation static mode and dynamic mode. Static mode achieves low power dissipation and dynamic mode achieves faster operation. Static power dissipation occurs due to leakage current and sub threshold current. In DML which provide designer with very high level of flexibility .Different types of researches are done for DFT. In power switches possibly there are two types of faults are occurred, Stuck short and stuck open fault .Stuck open fault are due to drain or source of the transistor is disconnected showing faulty behaviour. Stuck short means there is a direct connection between VDD and ground. It can be detected by IDDQ testing. The power switches are divided in to segments. The delay tests are used in both fine grain and coarse grain model.DFT solution suffer due to long discharging of transistor. In stuck at fault either logic 0 or logic 1 is present in the input and output lines. Single and multiple stuck at faults are occurred in logic circuits diagnosis is a systematic method for identifying faulty power switches. Fault means an error causing malfunction. Here only discuss about stuck at and stuck open fault. Be siding this fault bridging fault are exists. Single and multiple faults are occurred in the same logic design.

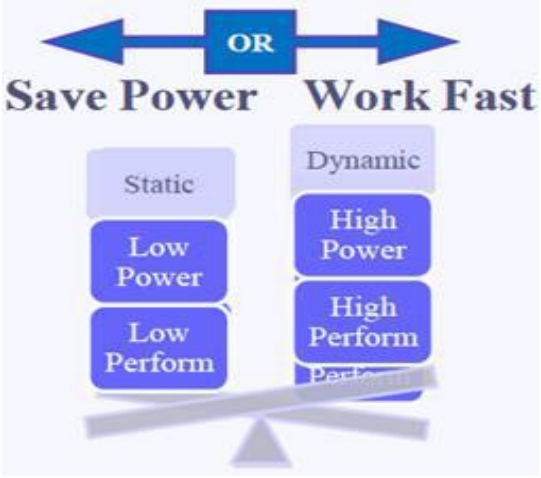


Fig 1.static and dynamic modes of operation

2. DML OVERVIEW

The digital circuits are the important blocks in integrated circuits. Hence the choice of cmos is sufficient. Two types of cmos 1) pmos and2) nmos Static mode of circuit use both cmos and nmos devices. A static gate having one or more logic inputs, a single logic output and a switching element that is associated with the static gate as shown in Fig. 2. The switching element comprises of an input that is connected to a

Constant voltage, and another input for providing a signal used for mode selection, an output that is connected to a logic output of the static gate. The switching element can be configured to operate in either of the two modes by: i) disconnecting the static gate output from both the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a constant voltage to the input used for providing mode selection signal, thereby selecting static mode of operation ii) Connecting the static gate output to both

the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a dynamic clock signal to the input used for providing mode selection signal, thereby to select dynamic mode operation.

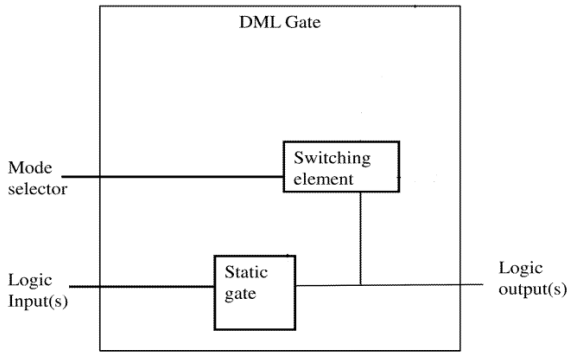


Fig 2.Basic DML gate

3. ANAALYSIS OF FINE GRAIN AND COARSE GRAIN

Power gating technique is used to reduce leakage current. There are two types of technique for power gating viz fine grain and coarse grain. In fine grain it in cooperates power switch within each standard logic cell with a control signal to switch on or off of the power supply of the cell. In coarse grain model a number of power switches are combined to feed back logic. The main drawback of fine grain is it utilizes maximum area compared with coarse grain. Fig 3 illustrates the fine grain design.

In this diagram control logic is used to control the test sequence. Multiplexers are used to enable standby mode or testing mode. Logic block help to save power by shutting unwanted blocks. The final output reaches at the NAND gate which shows fault response of the circuit. Coarse grain model DML parallel reduces delay compared with coarse grain model DML.

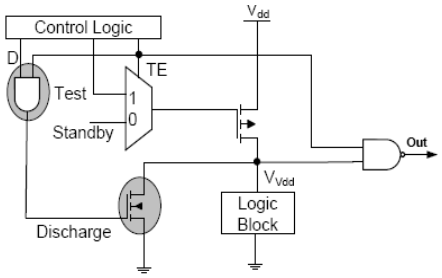


Fig 3. Fine grain model for power switches

4. DML GATE WITH POWER GATING

In coarse grain model DML gate is implemented in segments. mode selector select which mode of operation either static or dynamic. When they are alternatively switched to obtain better performance .power gating technique reduces the leakage power of the static mode of operation. in dynamic mode faster switching performance is obtained.

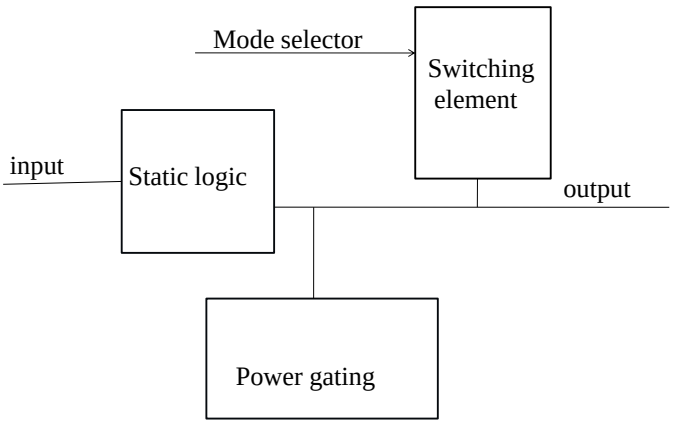


Fig 4 DML with power gating

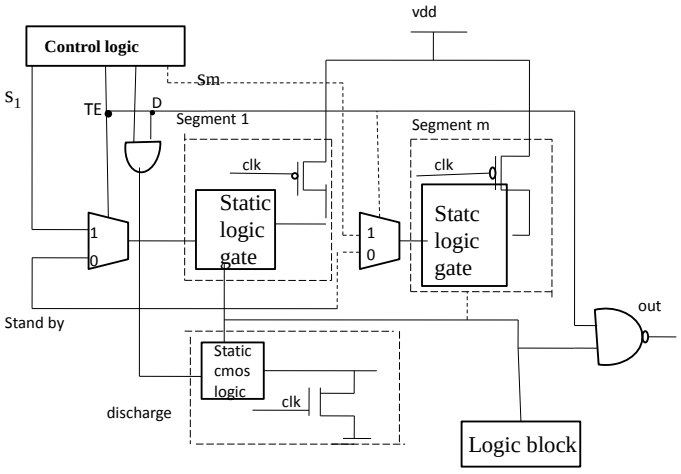


Fig 5 coarse grain with DML

5. ANALYSIS OF SEGMENT SIZE AND TEST FRQUENCY

In coarse grain DML model the control logic is used for controlling the test sequence. A multiplexer is used to enable test mode. The AND gate is used to control the discharging of transistor. The output of NAND gate shows fault response of the circuit.

The logic block consists of ISCAS bench marks designs that are synthesized using 90 nm gate libraries. The operating voltage used in this experiment is high. In coarse grain design style power switches are divided in to segments. And the number of power switches per segments has a tradeoff between area over head, test time and precision in identifying faulty transistor.

For a design shown in figure (5) segments consist of 5 power switches. We first stimulated test frequency and enable the test mode TE=1. D for controlling he discharging of transistor is set to zero, The power switches with DML is turned on and the fall time of the output of the NAND gate is observed when it reaches 20% of Vdd . This fall time is used to determine the test frequency. Hence we can determine maximum number of power switches per segment. Segment size varies from 5 to 30. We can extend the segment size more than 30.

Another factor effecting diagnosis accuracy of power switches is that test frequency. The number of detectable power switches is used to calculate diagnosis accuracy.

6. RESULTS AND DISCUSSIONS

TABE1 : Trade off:diagnosis accuracy and segment size

Design	Total ps	Segment size	Detectable ps	Diagnosis accuracy
C432	30	5	5	100%
		10	9	90%
		15	13	86%
		30	25	83%
C1908	120	5	5	100%
		10	9	90%
		15	14	93%
		30	25	83%
C2670	180	5	5	100%
		10	10	100%
		15	15	100%
		30	27	90%

F1,f

7. DIAGNOSIS ALGORITHM

Input: (net list m,f1,f2,f3,f4)

Where m is the total number of segment size .

F1,f2,f3,f4 are the test frequencies

Output:Faulty segments with number of power switches

1.TE=1

// TE is test enable

2.FF1=f1;FF2=f2

// FF is the frequency at which segment fails and used to determine the faulty power switches

3.D=1

// Enable discharge transistor

4. Si=1

//m is the total number of segment.

i=1

//I points to the first segment

6. repeat

7. TF=f1

// TF is the test frequency

8. si=0,D=0

// Turn on all segments at a time.

9. if out==0 then

// si is fault free

10. Else

Use lower test frequencies.(f2,f3andf4)to determine the number of faulty power switches.

11. push (I,FF1,FF2)

// Push on stack failed segment and the number of faulty power switches

12. end if

13. Si=1; d=1

14. i++

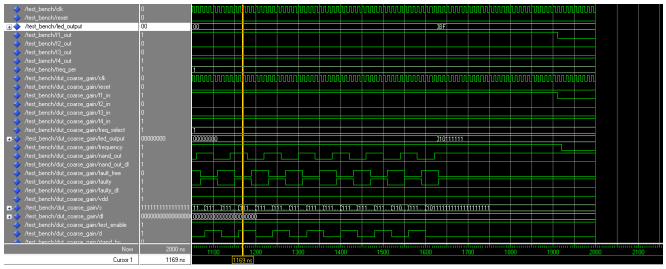
15.Untili<= m

16.return

8. CONCLUSION

By using model sim software the simulation results are verified. By using ISCAS benchmarks synthesized in 85 nm gate library. Simulation result is verified using test bench waveform. Under different test frequency are tested for better diagnosis accuracy.

Fig(6) coarse grain dml parallel model simulation



Fig(7) coarse grain model with DML

Table2:Timing report of DML and DML parallel

Timing report	Dml	Dml parallel
Maximum period	6.781ns	6.647ns
Maximum input arrival before clock	6.613ns	4.790ns
Maximum output time required after clock	4.283ns	4.203ns

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